WHAT IS CLAIMED IS:

1. A method of fabricating a shallow trench isolation structure of semiconductor device comprising:

forming a pad oxide layer and a first nitride layer on a substrate;

forming a trench by etching at least a portion of the first nitride layer, the pad oxide layer, and the substrate;

depositing an oxide layer and a second nitride layer on exposed surfaces of the first nitride layer, the pad oxide layer and the substrate including the trench;

forming a spacer on lateral walls of the trench by etching the second nitride layer;

growing a buried oxide in the substrate underneath the trench;

filling the trench by depositing an insulating layer after removing the spacer; and

performing a planarization process.

2. The method as defined by claim 1, wherein the oxide layer has a thickness of 225Å to 325Å.

3. The method according to claim 1, wherein the second nitride layer has a thickness of 250Å to 350Å.

4. The method as defined by claim 1, wherein the spacer is formed by etching the second nitride layer.

5. The method according to claim 4, wherein the spacer is formed by blanket etching the second nitride layer.

6. The method as defined by claim 1, wherein the buried oxide is formed underneath the trench and has a larger width than that of the trench.

7. The method according to claim 6, wherein the buried oxide has an oval shape.

8. The method according to claim 1, wherein the substrate is etched to an adequate depth.

9. The method according to claim 8, wherein the adequate depth is approximately 2000Å.

10. The method as defined by claim 1, wherein the trench is formed so as to have the same depth as source/drain regions.

11. The method as defined by claim 1, wherein the buried oxide is formed such that an adequate space exists between the buried oxide and another adjacent buried oxide.

12. The method according to claim 1, wherein the buried oxide is grown by performing a thermal oxidation on the substrate.

13. The method as defined by claim 12, wherein the thermal oxidation to form the buried oxide is a wet oxidation.

14. A shallow trench isolation structure of semiconductor device comprising:

a trench formed on an isolation area of a substrate;

an oxide formed on the lateral walls of the trench;

an insulating layer formed in the trench; and

a buried oxide formed underneath the trench, wherein the buried oxide having a larger width than a width of the trench.

15. The shallow trench isolation structure as defined by claim 14, wherein the buried oxide has an oval shape.

16. The shallow trench isolation structure as defined by claim 14, wherein the trench is formed so as to have a depth approximately equal to the depth of the source/drain regions.

17. The shallow trench isolation structure as defined by claim 14, wherein the buried oxide is formed such that an adequate space exists between the buried oxide and another adjacent buried oxide.